

SYSTÈME DE VIDÉOSURVEILLANCE

Dossier de Documentation Technique : DT

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Digital Thermometer and Thermostat

The DS1620 measures temperature using a bandgap-based temperature sensor. The temperature reading is provided in a 9-bit, two's complement reading by issuing a READ TEMPERATURE command. The data is transmitted serially through the 3-wire serial interface, LSB first. The DS1620 can measure temperature over the range of -55°C to +125°C in 0.5°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

Since data is transmitted over the 3-wire bus LSB first, temperature data can be written to/read from the DS1620 as either a 9-bit word (taking RST low after the 9th (MSB) bit), or as two transfers of 8-bit words, with the most significant 7 bits being ignored or set to 0, as illustrated in Table 3. After the MSB, the DS1620 will output 0s.

Note that temperature is represented in the DS1620 in terms of a ½°C LSB, yielding the 9-bit format shown in Figure 2.

TEMPERATURE, TH, and TL REGISTER FORMAT Figure 2

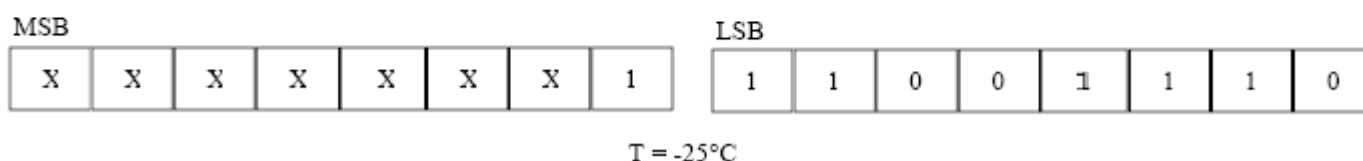


Table 3 describes the exact relationship of output data to measured temperature.

TEMPERATURE/DATA RELATIONSHIPS Table 3

TEMP	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	0 11111010	00FA
+25°C	0 00110010	0032h
+½°C	0 00000001	0001h
+0°C	0 00000000	0000h
-½°C	1 11111111	01FFh
-25°C	1 11001110	01CEh
-55°C	1 10010010	0192h

OPERATION—THERMOSTAT CONTROLS

Three thermally triggered outputs, T_{HIGH}, T_{LOW}, and T_{COM}, are provided to allow the DS1620 to be used as a thermostat, as shown in Figure 3. When the DS1620's temperature meets or exceeds the value stored in the high temperature trip register, the output T_{HIGH} becomes active (high) and remains active until the DS1620's measured temperature becomes less than the stored value in the high temperature register, TH.

The T_{LOW} output functions similarly to the T_{HIGH} output. When the DS1620's measured temperature equals or falls below the value stored in the low temperature register, the T_{LOW} output becomes active. T_{LOW} remains active until the DS1620's temperature becomes greater than the value stored in the low temperature register, TL.

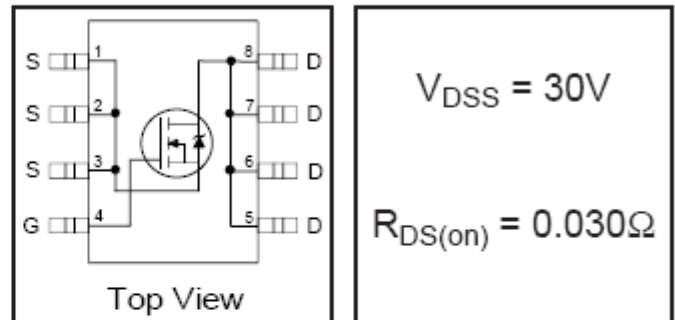
The T_{COM} output goes high when the measured temperature meets or exceeds TH, and will stay high until the temperature equals or falls below TL. In this way, any amount of hysteresis can be obtained.

- Generation V Technology
- Ultra Low On-Resistance
- N-Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching

Description

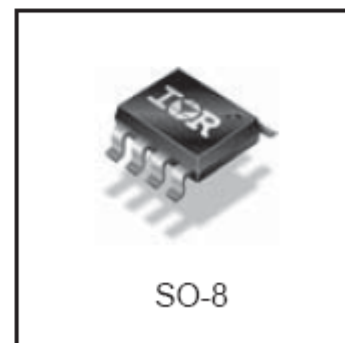
Fifth Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



$$V_{DSS} = 30V$$

$$R_{DS(on)} = 0.030\Omega$$



IRF7201

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions	
$V_{(BR)DSS}$	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$	
$\Delta V_{(BR)DSS}/\Delta T_J$	—	0.024	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$	
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.030	Ω	$V_{GS} = 10V, I_D = 7.3A$ ④
		—	—	0.050		$V_{GS} = 4.5V, I_D = 3.7A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$	
g_{fs}	Forward Transconductance	5.8	—	S	$V_{DS} = 15V, I_D = 2.3A$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	25		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
Q_g	Total Gate Charge	—	19	28	nC	$I_D = 4.6A$
Q_{gs}	Gate-to-Source Charge	—	2.3	3.5		$V_{DS} = 24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	6.3	9.5		$V_{GS} = 10V$, See Fig. 10 ④
$t_{d(on)}$	Turn-On Delay Time	—	7.0	—	ns	$V_{DD} = 15V$
t_r	Rise Time	—	35	—		$I_D = 4.6A$
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		$R_G = 6.2\Omega$
t_f	Fall Time	—	19	—		$R_D = 3.2\Omega$, ④
C_{iss}	Input Capacitance	—	550	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	260	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	100	—		$f = 1.0MHz$, See Fig. 9

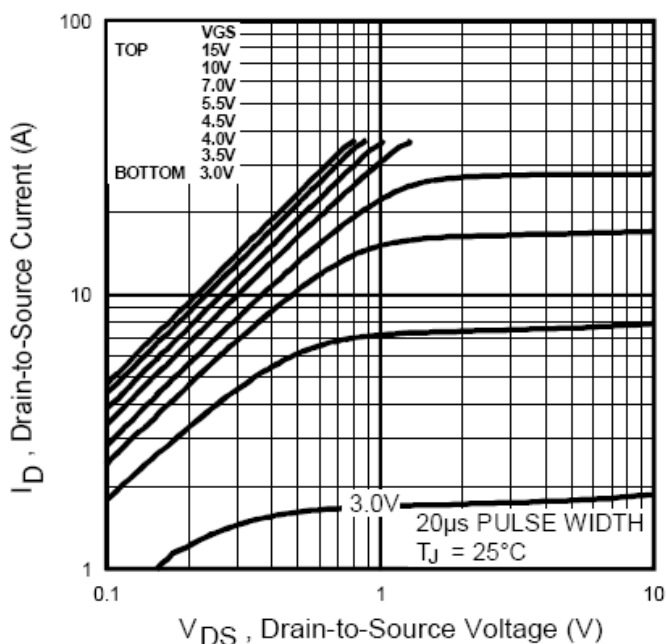


Fig 1. Typical Output Characteristics

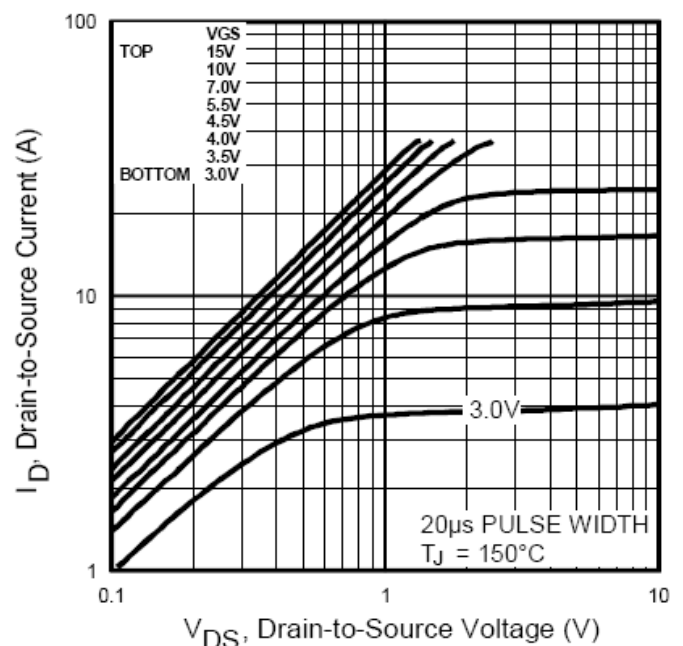
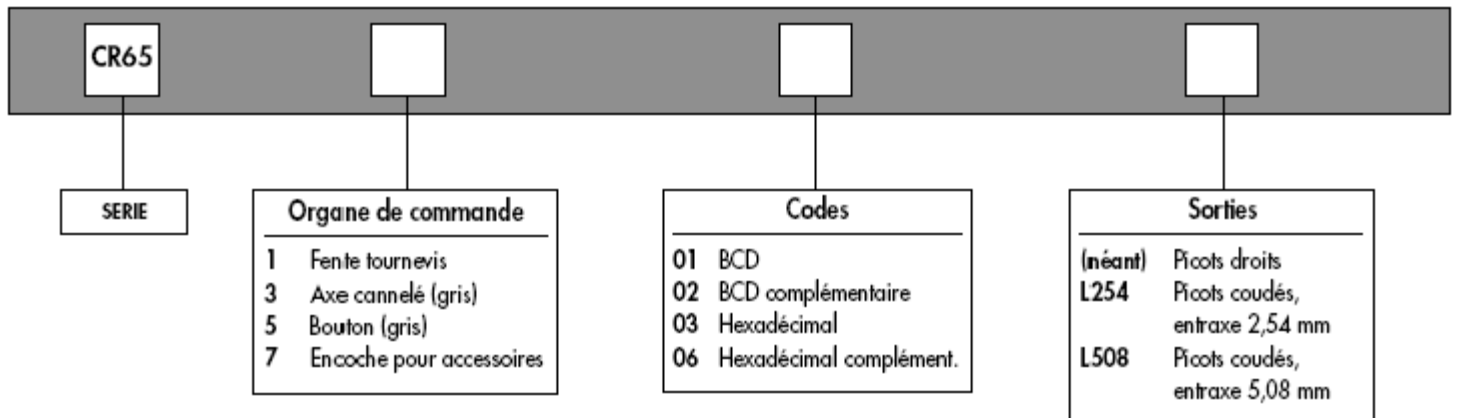
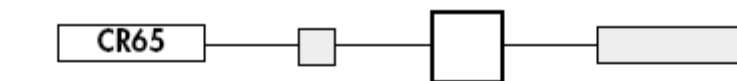


Fig 2. Typical Output Characteristics

COMMUTATEURS ROTATIFS DE CODAGE CR65



CODES / TABLES DE VERITE



01	BCD					
	C	1	2	4	8	
0	●					0
1	●	●				1
2	●		●			2
3	●	●	●			3
4	●			●		4
5	●	●		●		5
6	●		●	●		6
7	●	●	●	●		7
8	●				●	8
9	●	●			●	9

▲ Position du curseur

▲ Marquage

CARACTERISTIQUES ELECTRIQUES

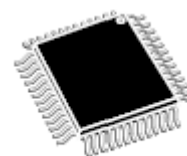
- Tension commutée : 24 V_{cc} maxi.
- Charge des contacts : 400mA maxi.
- Intensité commutée : 150mA maxi.
- Résistance de contact initiale : 80 mΩ maxi.
- Résistance d'isolement : 100 MΩ mini.

Sur une ligne les points indiquent les broches qui sont reliées entre elles

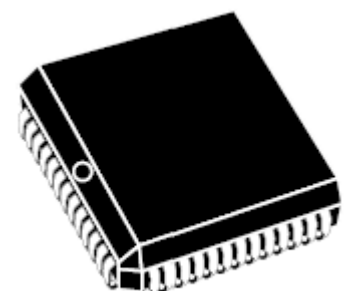
PSD813F1-A

FEATURES SUMMARY

- Single Supply Voltage:
 - 5 V \pm 10% for PSD813F1-A
 - 3.3 V \pm 10% for PSD813F1-AV
- Up to 1Mbit of Primary Flash Memory (8 uniform sectors)
- 256Kbit Secondary EEPROM (4 uniform sectors)
- Up to 16Kbit SRAM
- Over 3,000 Gates of PLD: DPLD and CPLD
- 27 Reconfigurable I/O ports
- Enhanced JTAG Serial Port
- Programmable power management
- High Endurance:
 - 100,000 Erase/Write Cycles of Flash Memory
 - 10,000 Erase/Write Cycles of EEPROM
 - 1,000 Erase/Write Cycles of PLD



PQFP52 (T)



PLCC52 (K)

PSD813F1-A

PSD813F1-A

Preliminary

PSD813F1 DC Characteristics (5 V ± 10% Versions)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V _{IH}	High Level Input Voltage	4.5 V < V _{CC} < 5.5 V	2		V _{CC} +.5	V
V _{IL}	Low Level Input Voltage	4.5 V < V _{CC} < 5.5 V	-.5		0.8	V
V _{IH1}	Reset High Level Input Voltage	(Note 1)	.8 V _{CC}		V _{CC} +.5	V
V _{IL1}	Reset Low Level Input Voltage	(Note 1)	-.5		.2 V _{CC} -.1	V
V _{HYS}	Reset Pin Hysteresis		0.3			V
V _{LKO}	V _{CC} Min for Flash Erase and Program		2.5		4.2	V
V _{OL}	Output Low Voltage	I _{OL} = 20 μA, V _{CC} = 4.5 V		0.01	0.1	V
		I _{OL} = 8 mA, V _{CC} = 4.5 V		0.25	0.45	V
V _{OH}	Output High Voltage Except V _{STBY} On	I _{OH} = -20 μA, V _{CC} = 4.5 V	4.4	4.49		V
		I _{OH} = -2 mA, V _{CC} = 4.5 V	2.4	3.9		V
V _{OH1}	Output High Voltage V _{STBY} On	I _{OH1} = 1 μA	V _{SBY} - 0.8			V
V _{SBY}	SRAM Standby Voltage		2.0		V _{CC}	V
I _{SBY}	SRAM Standby Current (V _{STBY} Pin)	V _{CC} = 0 V		0.5	1	μA
I _{IDLE}	Idle Current (V _{STBY} Pin)	V _{CC} > V _{SBY}	-0.1		0.1	μA
V _{DF}	SRAM Data Retention Voltage	Only on V _{STBY}	2			V
I _{SB}	Standby Supply Current for Power Down Mode	CSI > V _{CC} - 0.3 V (Notes 2 and 3)		50	200	μA
I _{LI}	Input Leakage Current	V _{SS} < V _{IN} < V _{CC}	-1	±1	1	μA
I _{LO}	Output Leakage Current	0.45 < V _{IN} < V _{CC}	-10	±5	10	μA

74HC4052

FUNCTION TABLE

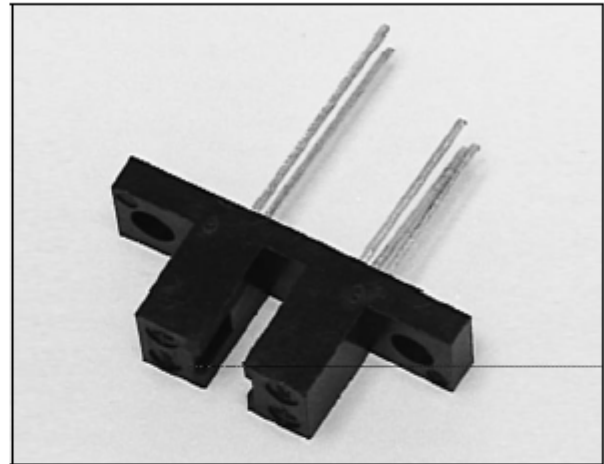
INPUT ⁽¹⁾			CHANNEL BETWEEN
\bar{E}	S1	S0	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

HOA2001

Transmissive Optoschmitt Sensor

FEATURES

- Direct TTL interface
- Buffer logic
- 0.060 in.(1.52 mm) dia. detector aperture
- 0.120 in.(3.05 mm) slot width
- 0.050 in.(1.27) offset pin circle detector eads



NFRA-45.TIF

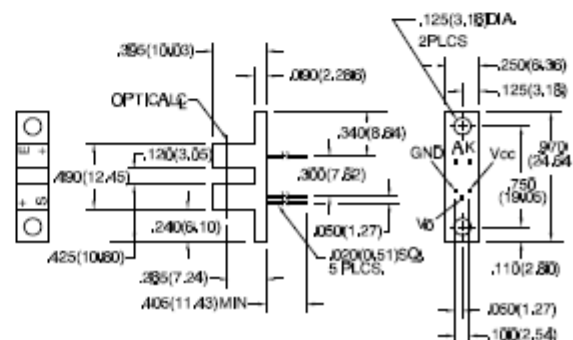
DESCRIPTION

The HOA2001 consists of an infrared emitting diode facing an Optoschmitt detector encased in a black thermoplastic housing. The photodetector consists of a photodiode, amplifier, voltage regulator, Schmitt trigger and an NPN output transistor with 10 k Ω (nominal) pull-up resistor. The buffer logic provides a high output when the optical path is clear, and a low output when the path is interrupted. The HOA2001 employs plastic molded components. For additional component information see SEP8506 and SDP8600.

Housing material is polyester. Housings are soluble in chlorinated hydrocarbons and ketones. Recommended cleaning agents are methanol and isopropanol.

OUTLINE DIMENSIONS in inches (mm)

Tolerance 3 plc decimals $\pm 0.010(0.25)$
2 plc decimals $\pm 0.020(0.51)$



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
IR EMITTER						
Forward Voltage	V_F			1.6	V	$I_F=20$ mA
Reverse Leakage Current	I_R			10	μ A	$V_R=3$ V
DETECTOR						
Operating Supply Voltage	V_{CC}	4.5		10	V	
Low Level Supply Current	I_{CCL}	4.0		12	mA	$V_{CC}=5$ V
Low Level Supply Current		5.0		15		$V_{CC}=12$ V
High Level Supply Current	I_{CCH}	2.0		10	mA	$V_{CC}=5$ V
High Level Supply Current		3.0		12		$V_{CC}=12$ V
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL}=12.8$ mA, $I_F=0$ mA
High Level Output Voltage	V_{OH}	2.4			V	$I_{OH}=0$, $I_F=10$ mA
Hysteresis ⁽²⁾	HYST		10		%	
Propagation Delay, Low-High	t_{PLH}		5		μ s	$V_{CC}=5$ V, $I_F=10$ mA
Propagation Delay, High-Low	t_{PHL}		5		μ s	$V_{CC}=5$ V, $I_F=10$ mA
Rise Time	t_r		60		ns	$R_L=390$ Ω , $C_L=50$ pF
Fall Time	t_f		15		ns	$R_L=390$ Ω , $C_L=50$ pF
COUPLED CHARACTERISTICS						
IRE Trigger Current HOA2001-001	I_{FT}			10	mA	$V_{CC}=5$ V

HOA2001

HOA2001

Transmissive Optoschmitt Sensor

ABSOLUTE MAXIMUM RATINGS

(25°C Free-Air Temperature unless otherwise noted)

Operating Temperature Range -40°C to 70°C

Storage Temperature Range -40°C to 85°C

Soldering Temperature (5 sec) 240°C

IR EMITTER

Power Dissipation 100 mW ⁽¹⁾

Reverse Voltage 3 V

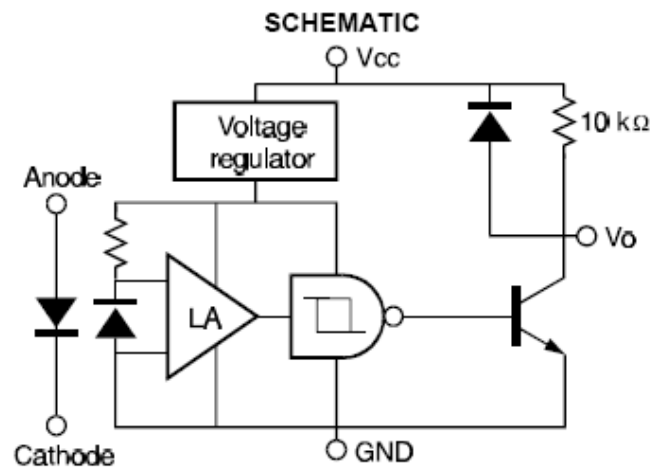
Continuous Forward Current 50 mA

DETECTOR

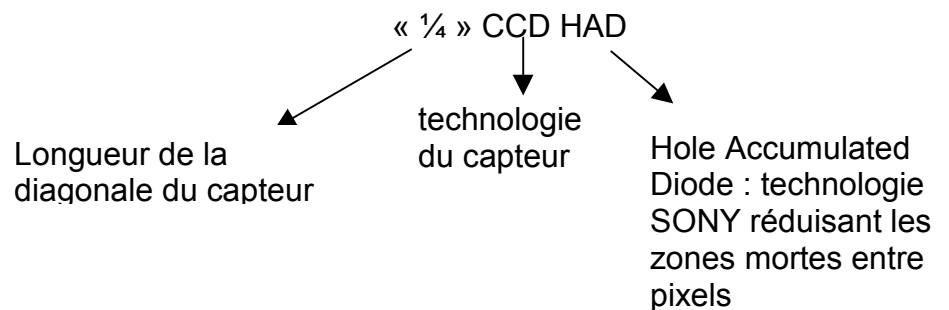
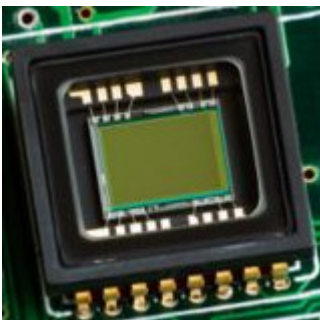
Supply Voltage 12 V ⁽²⁾

Output Sink Current 18 mA

Duration of Output Short to V_{CC} or Ground 1.0 sec.



Capteur CCD (*Charge-Coupled Device*, ou détecteurs à couplage de charge)



Un **capteur CCD** est un composant électronique servant à convertir un rayonnement (UV, visible ou IR) composé de photons en un signal électrique analogique. Ce signal sera ensuite numérisé par un convertisseur analogique numérique puis amplifié et traité pour obtenir une image numérique.

Le capteur CCD est constitué de cellules photosensibles appelées « photosites » qui transforment l'énergie lumineuse en charges électriques. Chaque photosite correspond à un point élémentaire de l'image appelé « pixel ». L'ensemble de ces photosites constitue une matrice active.

Low-Cost, μP Supervisory Circuits

General Description

The MAX705-MAX708/MAX813L microprocessor (μP) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in μP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX705/MAX706/MAX813L provide four functions:

- 1) A reset output during power-up, power-down, and brownout conditions.
- 2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6 seconds.
- 3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
- 4) An active-low manual-reset input.

The MAX707/MAX708 are the same as the MAX705/MAX706, except an active-high reset is substituted for the watchdog timer. The MAX813L is the same as the MAX705, except RESET is provided instead of $\overline{\text{RESET}}$.

Two supply-voltage monitor levels are available: The MAX705/MAX707/MAX813L generate a reset pulse when the supply voltage drops below 4.65V, while the MAX706/MAX708 generate a reset pulse below 4.40V. All four parts are available in 8-pin DIP, SO and μMAX packages.

Features

- ♦ μMAX Package: Smallest 8-Pin SO
- ♦ Guaranteed $\overline{\text{RESET}}$ Valid at $V_{CC} = 1V$
- ♦ Precision Supply-Voltage Monitor
4.65V in MAX705/MAX707/MAX813L
4.40V in MAX706/MAX708
- ♦ 200ms Reset Pulse Width
- ♦ Debounced TTL/CMOS-Compatible Manual-Reset Input
- ♦ Independent Watchdog Timer—1.6sec Timeout (MAX705/MAX706)
- ♦ Active-High Reset Output (MAX707/MAX708/MAX813L)
- ♦ Voltage Monitor for Power-Fail or Low-Battery Warning

Ordering Information

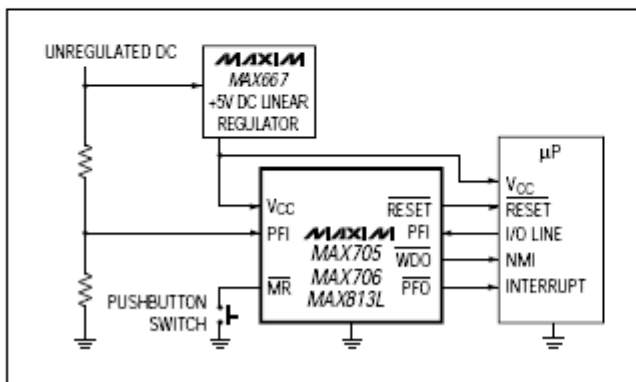
PART	TEMP. RANGE	PIN-PACKAGE
MAX705CPA	0°C to +70°C	8 Plastic DIP
MAX705CSA	0°C to +70°C	8 SO
MAX705CUA	0°C to +70°C	8 μMAX
MAX705C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

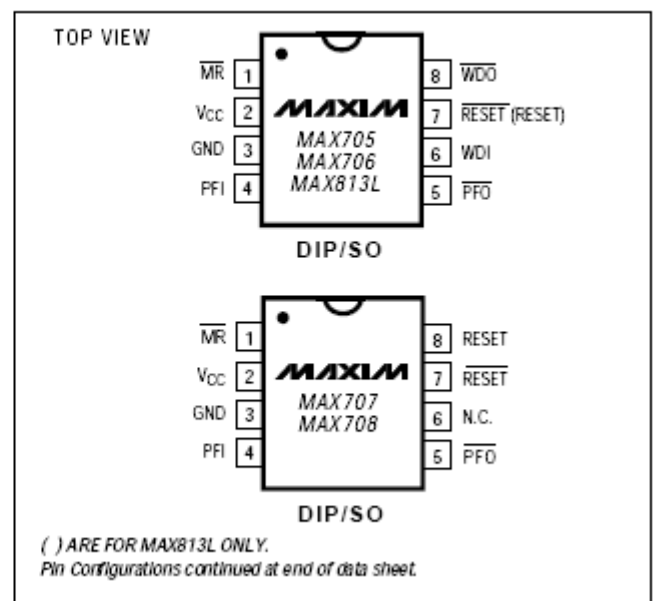
* Dice are specified at $T_A = +25^\circ\text{C}$.

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical μP Power Monitoring

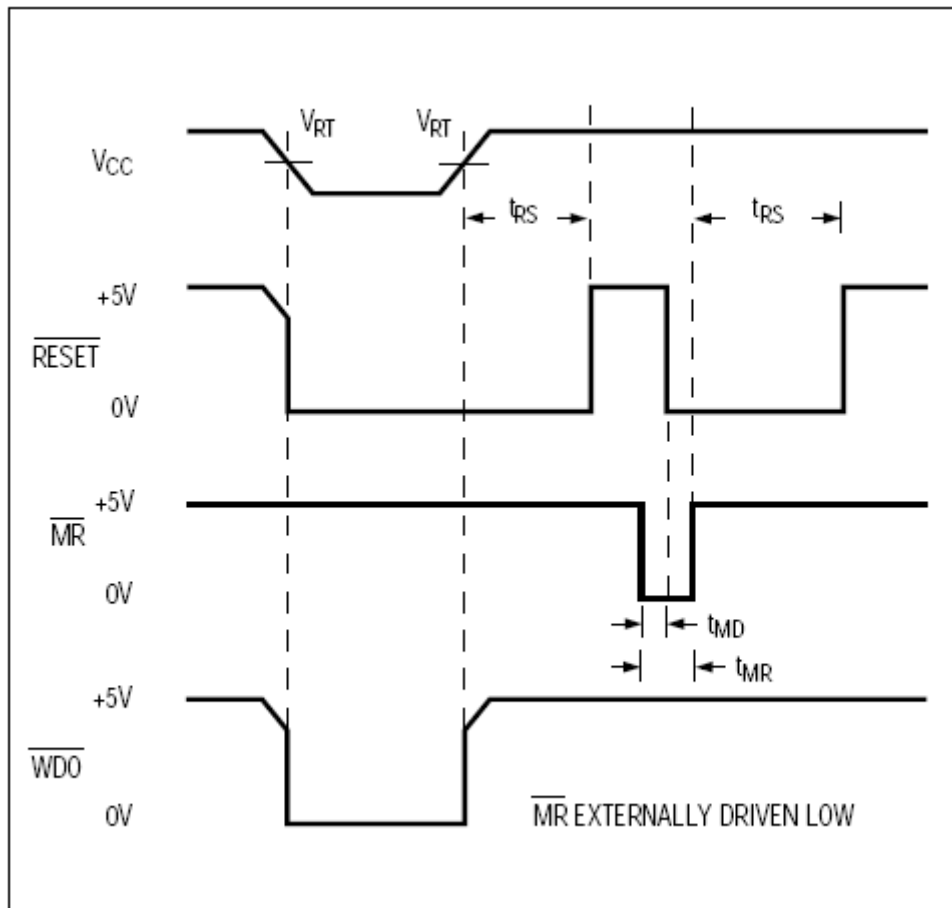
Typical Operating Circuit



Pin Configurations



MAX705



ELECTRICAL CHARACTERISTICS

($V_{CC} = 4.75V$ to $5.5V$ for MAX705/MAX707/MAX813L, $V_{CC} = 4.5V$ to $5.5V$ for MAX706/MAX708, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	MAX70_C	1.0		5.5	V
		MAX813LC	1.1		5.5	
		MAX70_E/M, MAX813LE/M	1.2		5.5	
Supply Current	I_{SUPPLY}	MAX705C, MAX706C, MAX813LC		150	350	μA
		MAX705E/M, MAX706E/M, MAX813LE/M		150	500	
		MAX707C, MAX708C		50	350	
		MAX707E/M, MAX708E/M		50	500	
Reset Threshold (Note 2)	V_{RT}	MAX705, MAX707, MAX813L	4.50	4.65	4.75	V
		MAX706, MAX708	4.25	4.40	4.50	
Reset Threshold Hysteresis (Note 2)				40		mV
Reset Pulse Width (Note 2)	t_{RS}		140	200	280	ms
\overline{RESET} Output Voltage		$I_{SOURCE} = 800\mu A$	$V_{CC} - 1.5$			V
		$I_{SINK} = 3.2mA$			0.4	
		MAX70_C, $V_{CC} = 1V$, $I_{SINK} = 50\mu A$			0.3	
		MAX70_E/M, $V_{CC} = 1.2V$, $I_{SINK} = 100\mu A$			0.3	
RESET Output Voltage		MAX707, MAX708, $I_{SOURCE} = 800\mu A$	$V_{CC} - 1.5$			V
		MAX707, MAX708, $I_{SINK} = 1.2mA$			0.4	
		MAX813LC, $I_{SOURCE} = 4\mu A$, $V_{CC} = 1.1V$	0.8			
		MAX813LE/M, $I_{SOURCE} = 4\mu A$, $V_{CC} = 1.2V$	0.9			
		MAX813L	$I_{SOURCE} = 800\mu A$	$V_{CC} - 1.5$		
		$I_{SINK} = 3.2mA$			0.4	
Watchdog Timeout Period	t_{WD}	MAX705, MAX706, MAX813L	1.00	1.60	2.25	sec
WDI Pulse Width	t_{WP}	$V_{IL} = 0.4V$, $V_{IH} = (V_{CC}) (0.8)$	50			ns
WDI Input Threshold	Low	MAX705, MAX706, MAX813L, $V_{CC} = 5V$			0.8	V
	High		3.5			
WDI Input Current		MAX705, MAX706, MAX813L, $WDI = V_{CC}$	50	150		μA
		MAX705, MAX706, MAX813L, $WDI = 0V$	-150	-50		

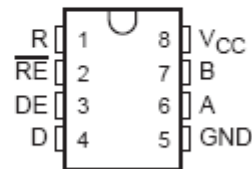
SN75176A

SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995

- Bidirectional Transceiver
- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and ITU Recommendation V.11
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ± 60 mA Max
- Thermal-Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedance . . . 12 k Ω Min
- Receiver Input Sensitivity . . . ± 200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From Single 5-V Supply
- Low Power Requirements

D OR P PACKAGE
(TOP VIEW)



description

The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The SN75176A combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 k Ω , an input sensitivity of ± 200 mV, and a typical input hysteresis of 50 mV.

The SN75176A can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN75176A is characterized for operation from 0°C to 70°C.

SN75176A

Function Tables

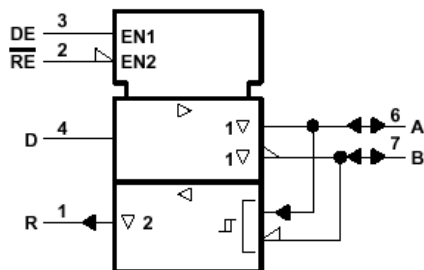
DRIVER			
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE \overline{RE}	OUTPUT R
$V_{ID} \geq 0.2 V$	L	H
$-0.2 V < V_{ID} < 0.2 V$	L	?
$V_{ID} \leq -0.2 V$	L	L
X	H	Z
Open	L	?

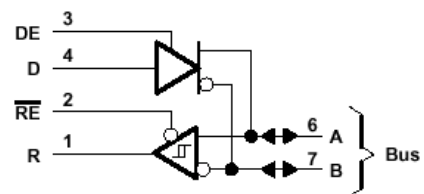
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74HC573

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	\overline{OE}	LE	D_N		Q_0 to Q_7
enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
latch and read register	L	L	l	L	L
	L	L	h	H	H
latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

ALE = LE (Broche 11)
/OE (Broche 1)

Notes

- H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state



PIC17C7XX

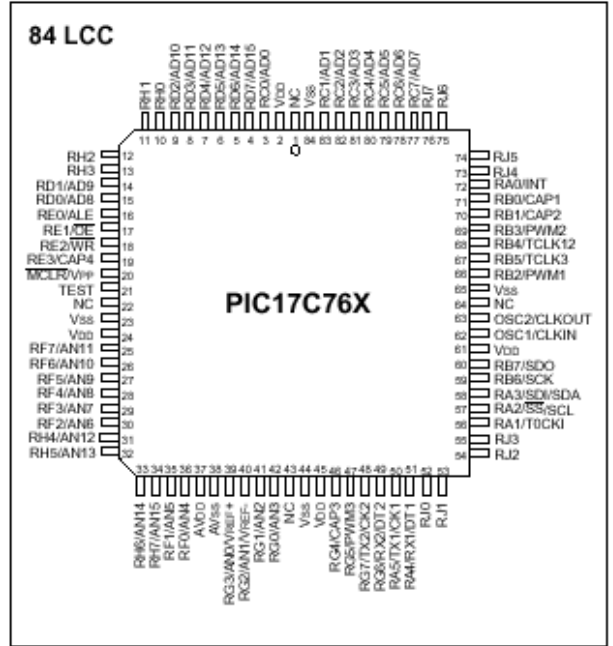
High-Performance 8-Bit CMOS EPROM Microcontrollers with 10-bit A/D

Microcontroller Core Features:

- Only 58 single word instructions to learn
- All single cycle instructions (121 ns) except for program branches and table reads/writes which are two-cycle
- Operating speed:
 - DC - 33 MHz clock input
 - DC - 121 ns instruction cycle
- 8 x 8 Single-Cycle Hardware Multiplier
- Interrupt capability
- 16 level deep hardware stack
- Direct, indirect, and relative addressing modes
- Internal/external program memory execution, Capable of addressing 64K x 16 program memory space

Device	Memory	
	Program (x16)	Data (x8)
PIC17C752	8K	678
PIC17C756A	16K	902

Pin Diagrams



Name	PIC17C75X			PIC17C76X		I/O/P Type	Buffer Type	Description
	DIP No.	PLCC No.	TQFP No.	PLCC No.	QFP No.			
OSC1/CLKIN	47	50	39	62	49	I	ST	Oscillator input in crystal/resonator or RC oscillator mode. External clock input in external clock mode.
OSC2/CLKOUT	48	51	40	63	50	O	—	Oscillator output. Connects to crystal or resonator in crystal oscillator mode. In RC oscillator or external clock modes OSC2 pin outputs CLKOUT which has one fourth the frequency ($F_{osc}/4$) of OSC1 and denotes the instruction cycle rate.
MCLR/VPP	15	16	7	20	9	I/P	ST	Master clear (reset) input or Programming Voltage (VPP) input. This is the active low reset input to the device.
RA0/INT	56	60	48	72	58	I	ST	PORTA pins have individual differentiations that are listed in the following descriptions: RA0 can also be selected as an external interrupt input. Interrupt can be configured to be on positive or negative edge. Input only pin.

Legend: I = Input only; O = Output only; I/O = Input/Output;
P = Power; — = Not Used; TTL = TTL input; ST = Schmitt Trigger input.

Note 1: The output is only available by the peripheral operation.

2: Open Drain input/output pin. Pin forced to input upon any device reset.

PIC17C752

ADCON0 REGISTER (ADDRESS: 14h, BANK 5)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	
CHS3	CHS2	CHS1	CHS0	—	GO/DONE	—	ADON	
bit7								bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-4: **CHS3:CHS0**: Analog Channel Select bits
0000 = channel 0, (AN0)
0001 = channel 1, (AN1)
0010 = channel 2, (AN2)
0011 = channel 3, (AN3)
0100 = channel 4, (AN4)
0101 = channel 5, (AN5)
0110 = channel 6, (AN6)
0111 = channel 7, (AN7)
1000 = channel 8, (AN8)
1001 = channel 9, (AN9)
1010 = channel 10, (AN10)
1011 = channel 11, (AN11)
1100 = channel 12, (AN12) (PIC17C76X only)
1101 = channel 13, (AN13) (PIC17C76X only)
1110 = channel 14, (AN14) (PIC17C76X only)
1111 = channel 15, (AN15) (PIC17C76X only)
11xx = **RESERVED**, do not select (PIC17C75X only)

bit 3: **Unimplemented**: Read as '0'

bit 2: **GO/DONE**: A/D Conversion Status bit
If ADON = 1
1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
0 = A/D conversion not in progress

bit 1: **Unimplemented**: Read as '0'

bit 0: **ADON**: A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shutoff and consumes no operating current

Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires a minimum 12TAD per 10-bit conversion. The source of the A/D conversion clock is software selected. The four possible options for TAD are:

- 8Tosc
- 32Tosc
- 64Tosc
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 μs.

TAD vs. DEVICE OPERATING FREQUENCIES (STANDARD DEVICES (C))

AD Clock Source (TAD)		Device Frequency				
Operation	ADCS1:ADCS0	33 MHz	20 MHz	5 MHz	1.25 MHz	333.33 kHz
8Tosc	00	242 ns ⁽²⁾	400 ns ⁽²⁾	1.6 μs	6.4 μs	24 μs
32Tosc	01	970 ns ⁽²⁾	1.6 μs	6.4 μs	25.6 μs ⁽³⁾	96 μs ⁽³⁾
64Tosc	10	1.94 μs	3.2 μs	12.8 μs ⁽³⁾	51.2 μs ⁽³⁾	192 μs ⁽³⁾
RC	11	2 - 6 μs ^(1,4)	2 - 6 μs ^(1,4)	2 - 6 μs ^(1,4)	2 - 6 μs ^(1,4)	2 - 6 μs ⁽¹⁾

Legend: Shaded cells are outside of recommended ranges.

PIC17C752

ADCON1 REGISTER (ADDRESS 15h, BANK 5)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	ADFM	—	PCFG3	PCFG2	PCFG1	PCFG0

bit7

bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **ADCS1:ADCS0:** A/D Conversion Clock Select bits

- 00 = FOSC/8
- 01 = FOSC/32
- 10 = FOSC/64
- 11 = FRC (clock derived from an internal RC oscillator)

bit 5: **ADFM:** A/D Result format select

- 1 = Right justified. 6 Most Significant bits of ADRESH are read as '0'.
- 0 = Left justified. 6 Least Significant bits of ADRESL are read as '0'.

bit 4: **Unimplemented:** Read as '0'

bit 3-1: **PCFG3:PCFG1:** A/D Port Configuration Control bits

PCFG3:PCFG1	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
000	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
001	D	A	A	A	A	A	A	A	D	A	A	A	A	A	A	A
010	D	D	A	A	A	A	A	A	D	D	A	A	A	A	A	A
011	D	D	D	A	A	A	A	A	D	D	D	A	A	A	A	A
100	D	D	D	D	A	A	A	A	D	D	D	D	A	A	A	A
101	D	D	D	D	D	A	A	A	D	D	D	D	D	A	A	A
110	D	D	D	D	D	D	A	A	D	D	D	D	D	D	A	A
111	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

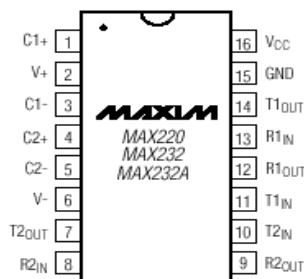
bit 0: **PCFG0:** A/D Voltage Reference Select bit

- 1 = A/D reference is the VREF+ and VREF- pins
- 0 = A/D reference is AVDD and AVSS

Note:When this bit is set, ensure that the A/D voltage reference specifications are met.

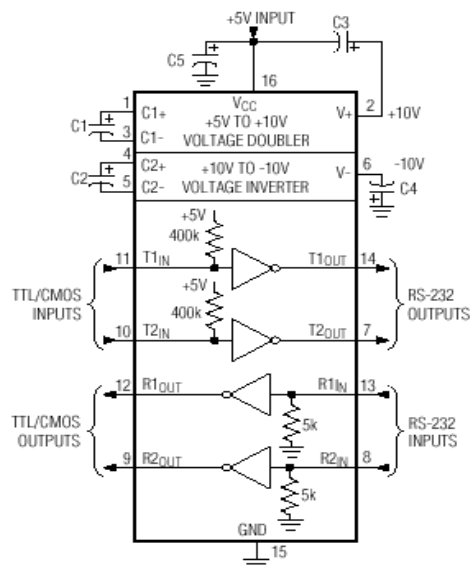
MAX232

TOP VIEW

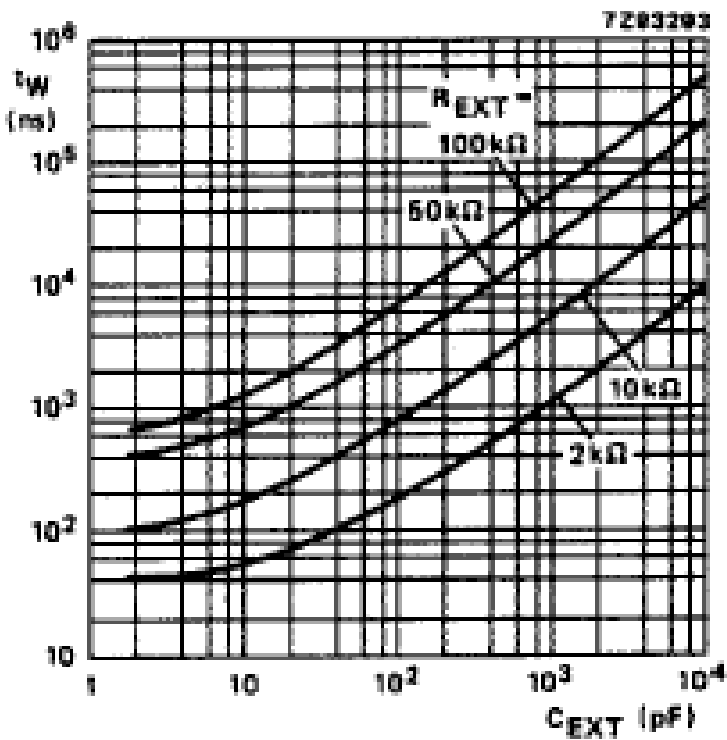


DIP/SO

DEVICE	C1	C2	C3	C4	C5
MAX220	4.7	4.7	10	10	4.7
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1



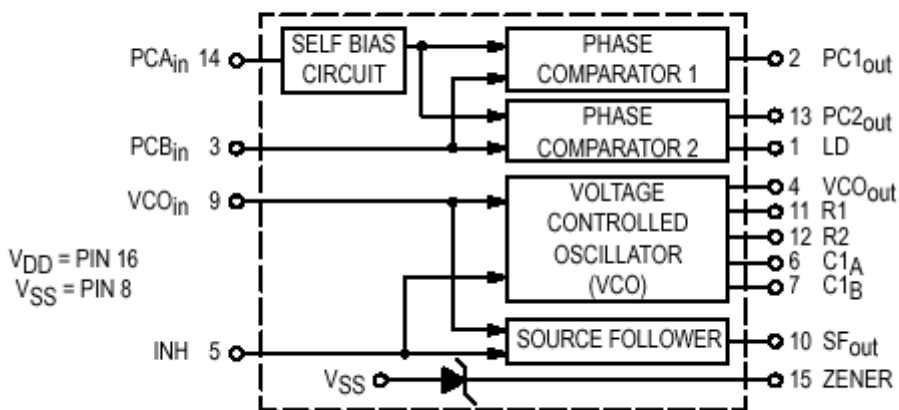
74HC123



If $C_{EXT} > 10\text{ nF}$, the next formula is valid:
 $tW = K \cdot R_{EXT} \cdot C_{EXT}$ (typ.)
 where: tW = output pulse width in ns;
 K = constant = 0.55 for $V_{CC} = 5.0\text{ V}$
 and 0.48 for $V_{CC} = 2.0\text{ V}$.

74HC4046

BLOCK DIAGRAM



COMMANDES PROTOCOLE ERNA

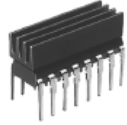
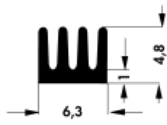
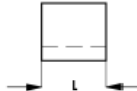

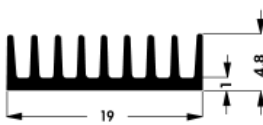
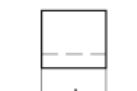
Command	Function	Data 1	Description	Data 2	Description	CS Type
1	Relays	0-255	Bit 0: Pan right Bit 1: Pan left Bit 2: Tilt up Bit 3: Tilt down Bit 4: Zoom wide Bit 5: Zoom tele Bit 6: Focus near Bit 7: Focus far	0-255	Bit 0: Iris open Bit 1: Iris close Bit 2: AUX1 Bit 3: AUX2 Bit 4: AUX3 Bit 5: AUX4 Bit 6: AUX5 Bit 7: AUX6	ALL
2	Call preposition	1-128	Prepos number	----	Not used	55X/575
3	Start Sequence prepos	0		----	Not used	55x/575/ICU
4	Text on/off	0		----	Not used	55x
5	Save prepos	1-128	Prepos number	----	Not used	55x/575/ICU
6	Insert prepos in stack	1-128	Prepos number	----	Not used	55x/575/ICU
7	Delete prepos from stack	1-128	Prepos number	----	Not used	55x/575/ICU
8	Clear seq. stack	0		----	Not used	55x/575/ICU
9	Show seq. stack	0		----	Not used	55x
10	Latch AUX	0-255	Bit 2: AUX1 Bit 3: AUX 2 Bit 4: AUX 3 Bit 5: AUX 4 Bit 6: AUX 5 Bit 7: AUX 6 Low=Latch High=No latch	----	Not used	51X/55x/ICU
11	Sequence dwelltime	0-255	Seconds	----	Not used	55x/575/ICU
12	Homefunction	0-253	Prepos number 0=Disabled	0-255	10x 1sec time-out	55x/575/ICU
		254	Auto Pan	----	Not used	ICU
		255	Sequence	----	Not used	ICU
13	AUX on/ off	1-8	Relay number	0-1	0=Off 1=On	55x/575/ICU
14	PT Speed	0-255	Pan Speed	0-255	Tilt Speed	575/ICU
15	Auto-paning	1	Speed	0-255		575/ICU
		2	Limits	1/2		
		3	Start	----	Not used	
16	Camera Set-up	1	Mode	0-255	Bit 0: Internal Bit 1: Remote	ICU
		2	Gain control.	0-255	0=low 255=high	
		3	White balance.	0-255	0=Warm 255=Cold	
		4	Contour corr.	0-255	0=Sharp 255=Soft	
		5	Shutter speed	0-255	0=Fast 255=Slow	
		6	Background comp.	----	Not used	
		7	Auto iris	0-255	Bit 0-3: ALC 0=Peak 8=Normal F=Average Bit 4-7: Level 0=Low 8=Normal F=High	ICU

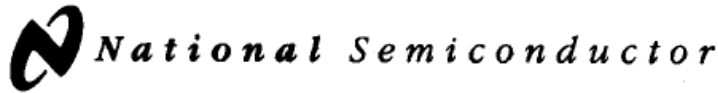
COMMANDES PROTOCOLE VISCA

Command Set	Command	Command Packet	Comments
AddressSet	Broadcast	88 30 01 FF	
IF_Clear	Broadcast	88 01 00 01 FF	
CommandCancel		8x 2p FF	p: Socket No.(=1or2)
CAM_Power	On	8x 01 04 00 02 FF	Power ON/OFF
	Off	8x 01 04 00 03 FF	
CAM_Zoom	Stop	8x 01 04 07 00 FF	p=0 (Low) to 7 (High) pqrs: Zoom Position
	Tele(Standard)	8x 01 04 07 02 FF	
	Wide(Standard)	8x 01 04 07 03 FF	
	Tele(Variable)	8x 01 04 07 2p FF	
	Wide(Variable)	8x 01 04 07 3p FF	
	Direct	8x 01 04 47 0p 0q 0r 0s FF	
CAM_DZoom	On	8x 01 04 06 02 FF	Digital zoom ON/OFF
	Off	8x 01 04 06 03 FF	
	Combine Mode	8x 01 04 36 00 FF	Optical/Digital Zoom Combined
	Separate Mode	8x 01 04 36 01 FF	Optical/Digital Zoom Separate
	Stop	8x 01 04 06 00 FF	
	Tele(Variable)	8x 01 04 06 2p FF	p=0 (Low) to 7 (High)
	Wide(Variable)	8x 01 04 06 3p FF	
	x1/Max	8x 01 04 06 10 FF	x1/MAX Magnification Switchover
	Direct	8x 01 04 46 00 0p 0q FF	pq: D-Zoom Position

DISSIPATEURS THERMIQUES

Heatsinks for DIL-IC

			
art. no.	R_{th} [K/W]	for housings	dim. [mm] L
ICK 14 16 L	46	14/16 contacts	19.0
ICK 20 L	34	20 contacts	25.0
ICK 6 8 L	83	6/8 contacts	8.5
			
art. no.	R_{th} [K/W]	for housings	dim. [mm] L
ICK 14 16 B	50.0	14/16 contacts	6.3
ICK 24 B	13.0	24 contacts	33.0



LM1881 Video Sync Separator

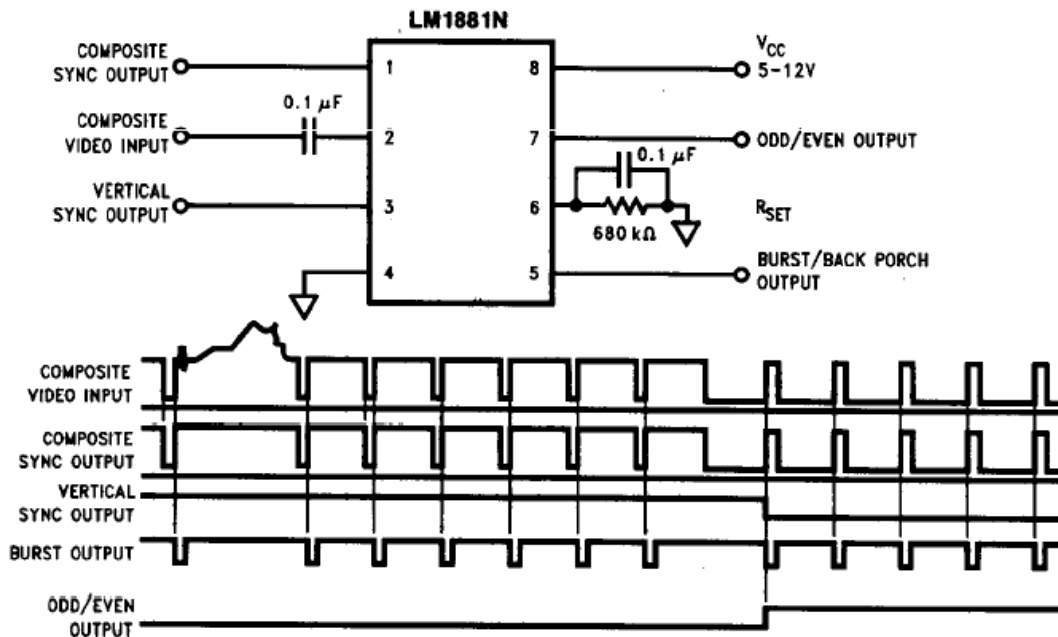
General Description

The LM1881 Video sync separator extracts timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from standard negative going sync NTSC, PAL*, and SECAM video signals with amplitude from 0.5V to 2V p-p. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the externally set delay period, such as might be the case for a non-standard video signal.

Features

- AC coupled composite input signal
- >10 k Ω input resistance
- <10 mA power supply drain current
- Composite sync and vertical outputs
- Odd/even field output
- Burst gate/back porch output
- Horizontal scan rates to 150 kHz
- Edge triggered vertical output
- Default triggered vertical output for non-standard video signal (video games-home computers)

Connection Diagram



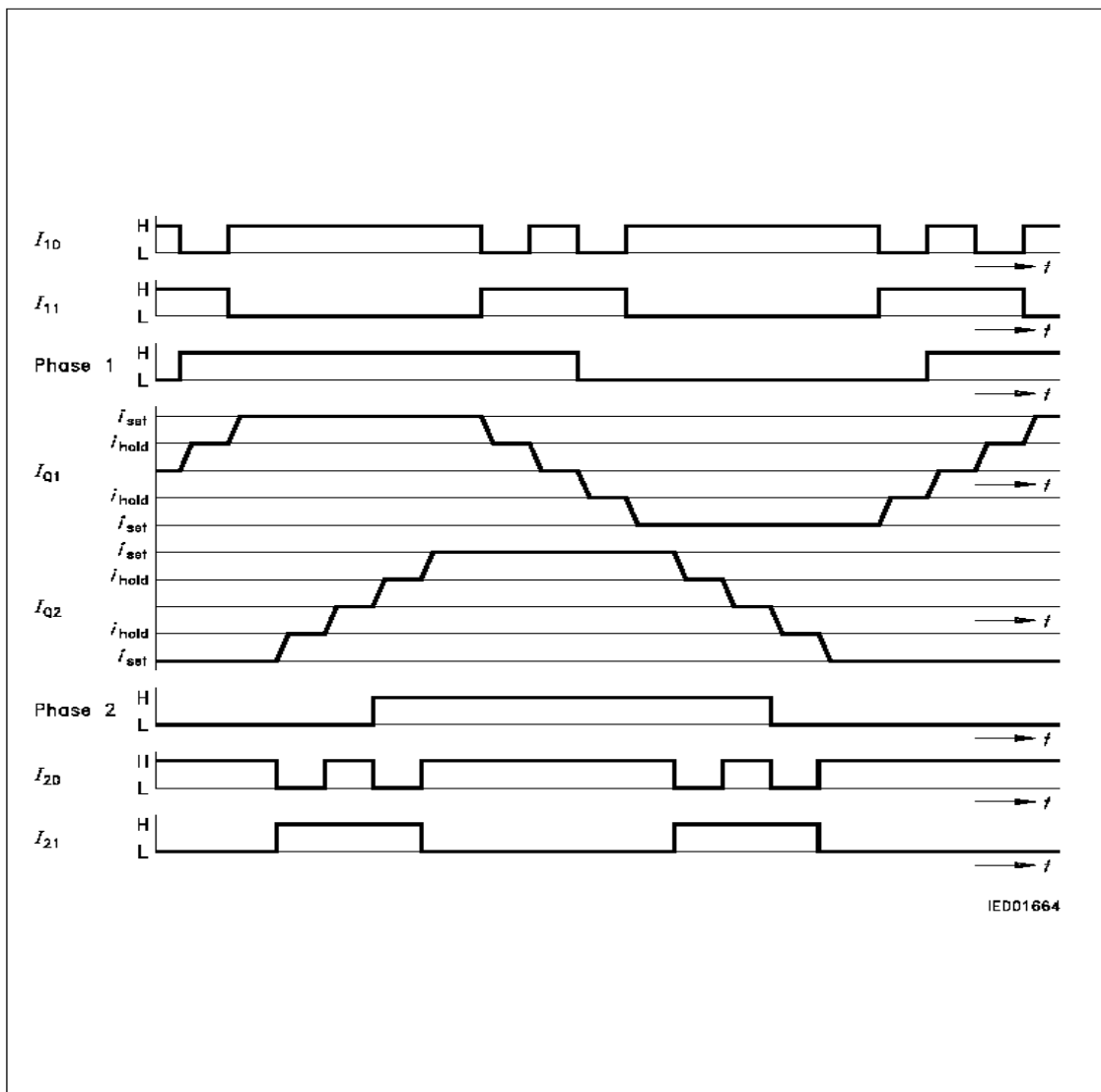
Order Number LM1881M or LM1881N
See NS Package Number M08A or N08E

TL/H/9150-1

TCA3727

Pin	Function																				
1, 2, 19, 20 (1, 2, 23, 24) ¹⁾	<p>Digital control inputs IX0, IX1 for the magnitude of the current of the particular phase.</p> <table border="1"> <thead> <tr> <th>IX1</th> <th>IX0</th> <th>Phase current</th> <th>Example of motor status</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>0</td> <td>No current</td> </tr> <tr> <td>H</td> <td>L</td> <td>$1/3 I_{max}$</td> <td>Hold</td> </tr> <tr> <td>L</td> <td>H</td> <td>$2/3 I_{max}$</td> <td>Set</td> </tr> <tr> <td>L</td> <td>L</td> <td>I_{max}</td> <td>Accelerate</td> </tr> </tbody> </table> <p style="text-align: right;">typical I_{max} with $R_{sense} = 1 \Omega : 750 \text{ mA}$</p>	IX1	IX0	Phase current	Example of motor status	H	H	0	No current	H	L	$1/3 I_{max}$	Hold	L	H	$2/3 I_{max}$	Set	L	L	I_{max}	Accelerate
IX1	IX0	Phase current	Example of motor status																		
H	H	0	No current																		
H	L	$1/3 I_{max}$	Hold																		
L	H	$2/3 I_{max}$	Set																		
L	L	I_{max}	Accelerate																		
3	Input Phase 1 ; controls the current through phase winding 1. On H-potential the phase current flows from Q11 to Q12, on L-potential in the reverse direction.																				
5, 6, 15, 16 (5, 6, 7, 8, 17, 18, 19, 20) ¹⁾	Ground ; all pins are connected internally.																				
4	Oscillator ; works at approx. 25 kHz if this pin is wired to ground across 2.2 nF.																				
8 (10) ¹⁾	Resistor R_1 for sensing the current in phase 1.																				
7, 10 (9, 12) ¹⁾	Push-pull outputs Q11, Q12 for phase 1 with integrated free-wheeling diodes.																				
9 (11) ¹⁾	Supply voltage ; block to ground, as close as possible to the IC, with a stable electrolytic capacitor of at least 10 μF in parallel with a ceramic capacitor of 220 nF.																				
12 (14) ¹⁾	Logic supply voltage ; either supply with 5 V or connect to + V_S across a series resistor. A Z-diode of approx. 7 V is integrated. In both cases block to ground directly on the IC with a stable electrolytic capacitor of 10 μF in parallel with a ceramic capacitor of 100 nF.																				
11, 14 (13, 16) ¹⁾	Push-pull outputs Q22, Q21 for phase 2 with integrated free wheeling diodes.																				
13 (15) ¹⁾	Resistor R_2 for sensing the current in phase 2.																				
17 (21) ¹⁾	Inhibit input ; the IC can be put on standby by low potential on this pin. This reduces the current consumption substantially.																				
18 (22) ¹⁾	Input phase 2 ; controls the current flow through phase winding 2. On H-potential the phase current flows from Q21 to Q22, on L potential in the reverse direction.																				

1) TCA 3727 G only



Quarter-Step Operation

Junction temperature max. : 125°C or 150°C (1000h)

Thermal resistance	Package
RTHj-a = 56 K/W	DIP - 20
RTHj-a = 75 K/W	DSO - 24
RTHj-c = 18 K/W	DIP - 20
RTHj-c = 15 K/W	DSO - 24

MOTEUR PAS A PAS

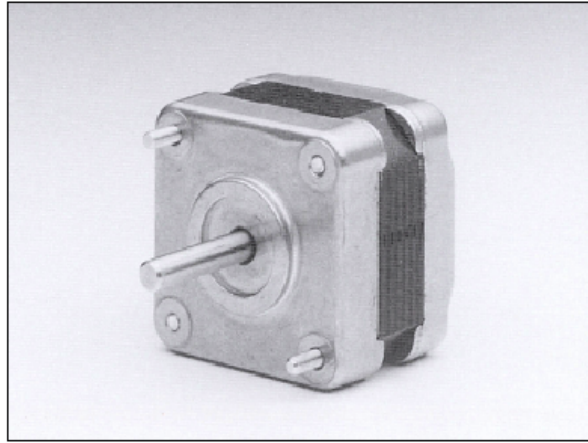
6540-13

**Angle de pas
Schrittwinkel
Step angle** 1.8 °

**Diamètre
Durchmesser
Diameter** 42 x 42 mm

**Poids
Gewicht
Weight** 200 g

**Couple de retenue
Haltemoment
Holding torque** 110/90 mNm



Pas Schritte/U Steps/rev	200
Précision/pas Schrittgenauigkeit Step accuracy	± 5 %
Inertie du rotor Rotorträgheitsmoment Rotor inertia	19 gcm²
Classe d'isolation Isolationsklasse Insulation class	B 130 °C
Protection Schutzart Protection	DIN 40050 IP 30
Tension d'essai Prüfspannung Test voltage	500 VAC
Couple résiduel Restmoment Detent torque	11 mNm

		Résistance de phase Phasenwiderstand Phase resistance Ω	Induct. de phase Phaseninduktivität Phase inductance mH	Courant de phase Phasenstrom Phase current A	Couple de retenue Haltemoment Holding torque mNm	Puissance nominale Nennleistung Nominal power W	
bipolar	6540-13-2-2	2	2	1.12	110	5	
	6540-13-2-9	9	9.5	0.52	110	5	
	6540-13-2-36	36	30	0.26	110	5	
unipolar	6540-13-4-2	2	1.1	1.12	90	5	
	6540-13-4-9	9	4.5	0.52	90	5	
	6540-13-4-36	36	17	0.26	90	5	

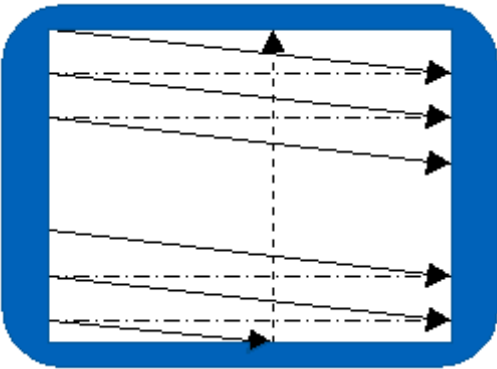
INFORMATIONS SUR LE SIGNAL VIDÉO COMPOSITE

A - LE STANDARD PAL

Dans le cas du **standard PAL**, il faut **625 lignes** pour constituer une image.
Le balayage d'une ligne dure 64 μ s.

Afin d'éviter l'effet observable de scintillement, on effectue un balayage « entrelacé » de l'écran : cela consiste à un balayage en deux « passes » ou trames consécutives comprenant :

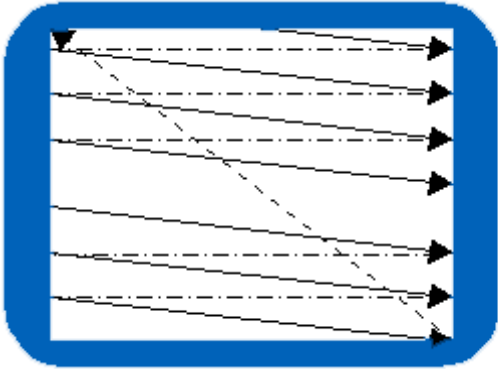
- les **lignes 1 à 288** (c'est la « **trame paire** »)
- un retour en haut de l'écran (équivalent à 25 lignes appelées « **lignes de retour trame** »)
- les **lignes 313 à 600** (c'est la « **trame impaire** »)
- à nouveau un retour en haut de l'écran (équivalent à 25 lignes appelées « **lignes de retour trame** »).



ligne 1
ligne 2
ligne 3

ligne 286
ligne 287
ligne 288

« Trame paire »



ligne 313
ligne 314
ligne 315

ligne 598
ligne 599
ligne 600

« Trame impaire »

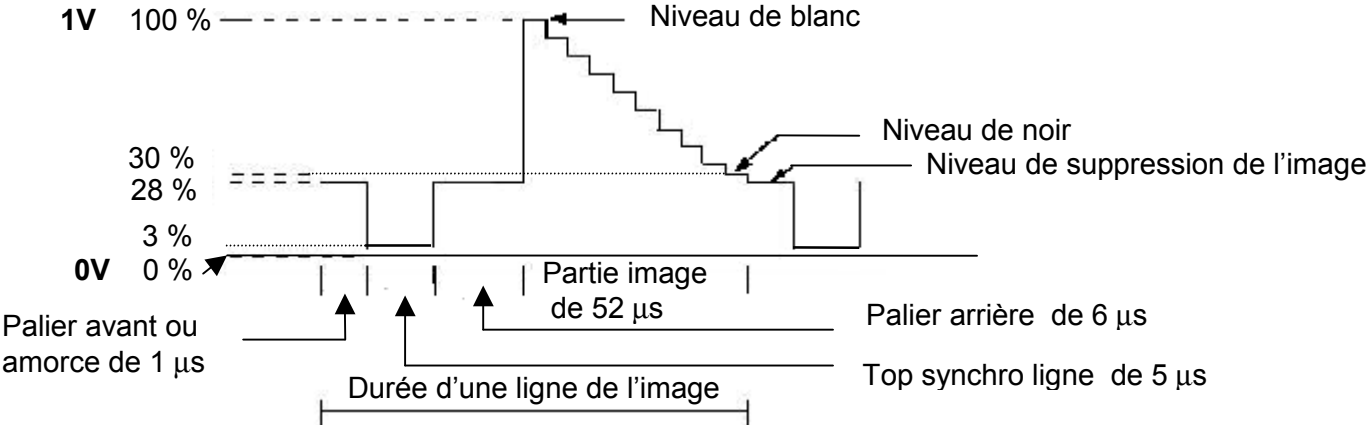
Les informations sur le signal vidéo composite données aux pages suivantes concernent le standard PAL.

B- LE SIGNAL VIDÉO COMPOSITE (À ASSOCIER À UNE LIGNE DE L'IMAGE)

Le **signal vidéo composite** correspondant à une ligne d'une image est composé :

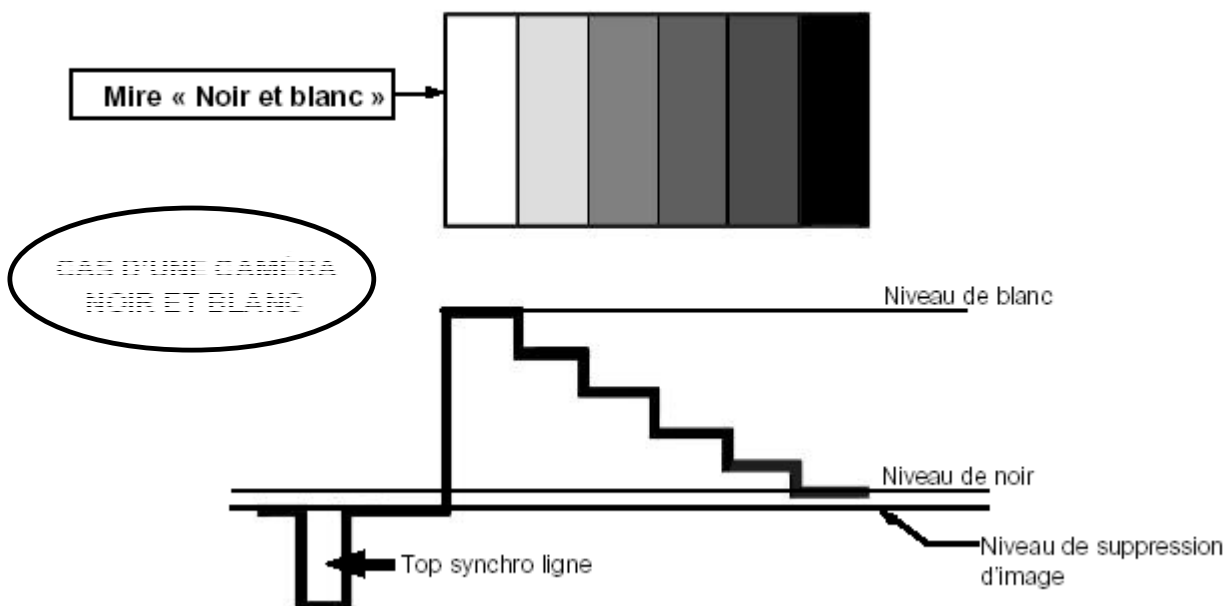
- d'une partie « synchronisation » indiquant le début d'une ligne de l'image
- d'une « partie image » définissant l'image proprement dite.

La figure ci-dessous donne les caractéristiques d'un signal vidéo composite au standard PAL « Noir et blanc »

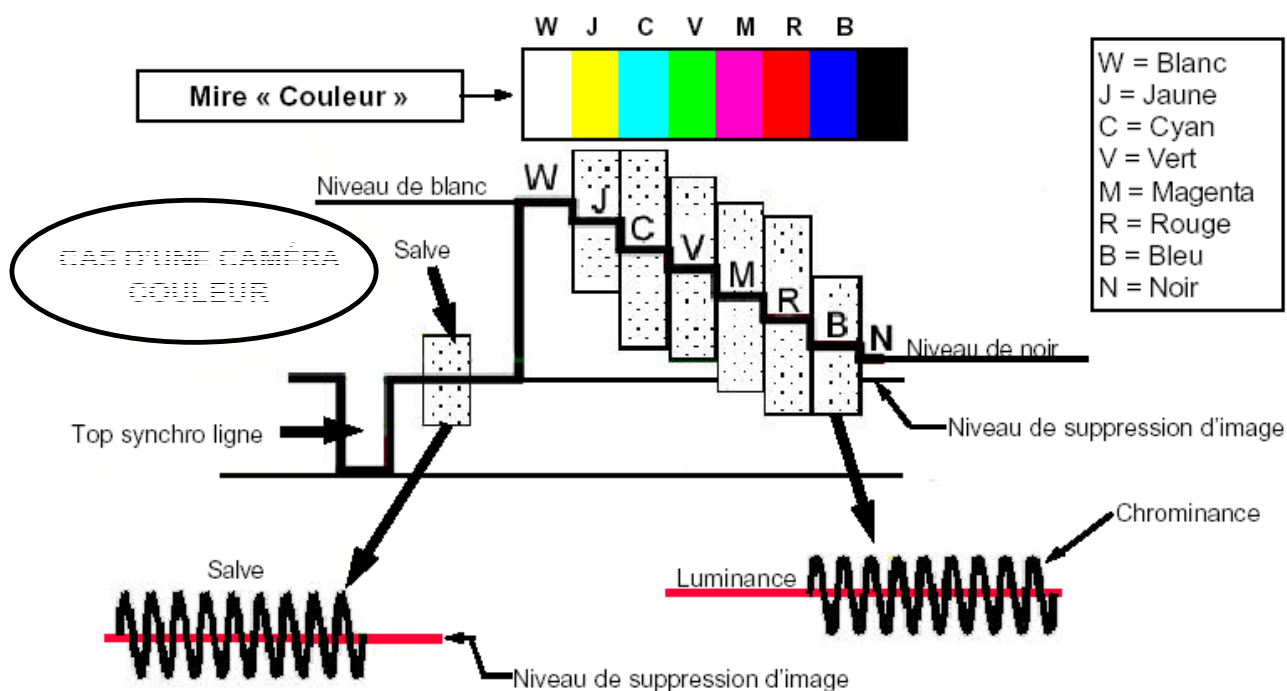


INFORMATIONS SUR LE SIGNAL VIDÉO COMPOSITE

D- SIGNAL VIDÉO COMPOSITE PAL « NOIR ET BLANC » ET MIRE ASSOCIÉE



E- SIGNAL VIDÉO COMPOSITE PAL « COULEUR » ET MIRE ASSOCIÉE



Remarque 1 : Le standard PAL « Couleur » est caractérisé par une salve présente sur le palier arrière du signal vidéo composite. Cette salve d'une durée d'environ 2,25 μ s et d'une amplitude de 300 mV est constituée par une dizaine de périodes (à 4,43 MHz).

Remarque 2 : Dans le standard PAL « Couleur », les couleurs sont matérialisées par l'apparition d'une modulation (chrominance) sur les différents paliers (luminance) du signal vidéo composite.